Bandgap References : Supply and Temperature Independent References

Analog Circuits Design I

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Outline

- MOSFET: Temperature dependence
- Supply-Independent Biasing
  - Power supply Sensitivity
  - Temperature sensitivity
- Temperature-Independent References
  - Negative-TC Ref(CTAT)
  - Positive-TC Ref (PTAT)
  - Band Gap Reference Design

MOSFET: Temperature dependence of V_T

- Many parameters of MOSFET vary with temperature, but two of them dominate: V_T and µ
- Threshold voltage is usually defined as the gate voltage for which the channel is as much n-type as the substrate is p-type resulting in:

$$V_{T0} = \phi_{ms} + 2\phi_B + \frac{Q_{dep}}{C_{ox}} = -\frac{k\boldsymbol{T}}{q}\ln\left(\frac{N_{D,poly}}{N_{sub}}\right) + \frac{Q_{dep}}{C_{ox}}$$

$$\frac{\partial V_T}{\partial T} \approx \underset{\uparrow}{-}\frac{k}{q}\ln\left(\frac{N_{D,poly}}{N_{sub}}\right) \quad with \quad \frac{k}{q} = \frac{\partial U_T}{\partial T} \approx 85\ \mu V/°C$$

ϕ_{ms} : is gate-substrate work functions difference

ϕ_B: electrostatic potential of the bulk (p-type substrate)

Q_{dep}: charge in the depletion region

$N_{D,poly}$: Doping concentration of the polysilicon gate

N_{sub}: Doping concentration of the substrate

- V_{T0} decreases when T increases

Ex. For $N_{D,poly}=10^{20}$ cm^{-3} and $N_{sub}=10^{17}$ cm^{-3}

$$\boxed{\rightarrow \frac{\partial V_T}{\partial T} \approx -0.6\, mV/°C}$$

- The temperature coefficient (relative variation) of V_{T0} (TC_{VT}) is defined as :

$$\boxed{TC_{VT} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} < 0}\ \boxed{\rightarrow V_T(T) = V_T(T_0)(1 + TC_{VT}\ (T - T_0))}$$

- The threshold voltage of a MOSFET exhibits a negative TC *(but defined with low accuracy)*

MOSFET: Temperature dependence of μ

- Due to thermal agitation, μ decreases when T increases (@ a first approximation) as:

$$\boxed{\mu(T) = \mu(T_0)\left(\frac{T_0}{T}\right)^{1.5}, T_0 = 300\ °\text{K}}$$

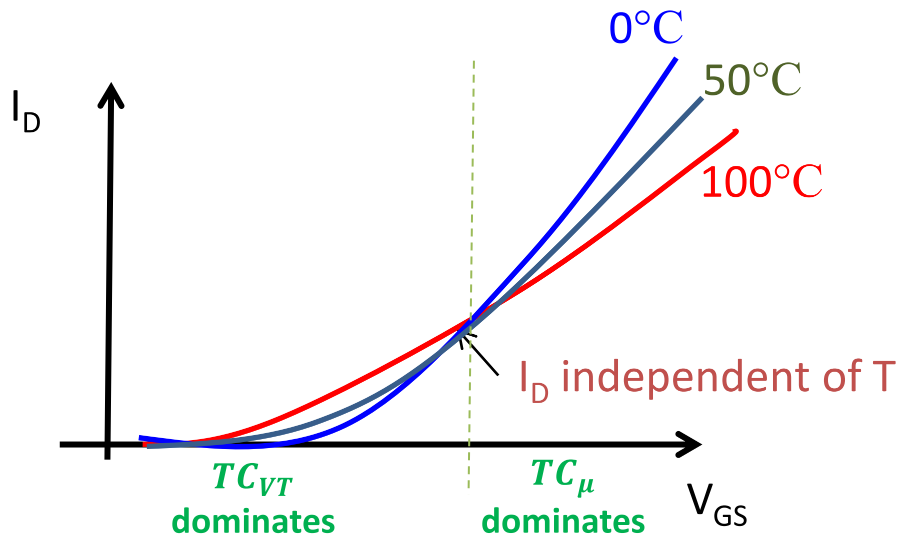
- The channel Mobility exhibits a negative TC

$$\rightarrow TC\mu(T) = \frac{1}{\mu(T)}\frac{\partial\mu(T)}{\partial T} \approx -\frac{1.5}{T}$$

and $\mu(T) = \mu(T_0)(1 - \frac{1.5}{T}(T - T_0))$

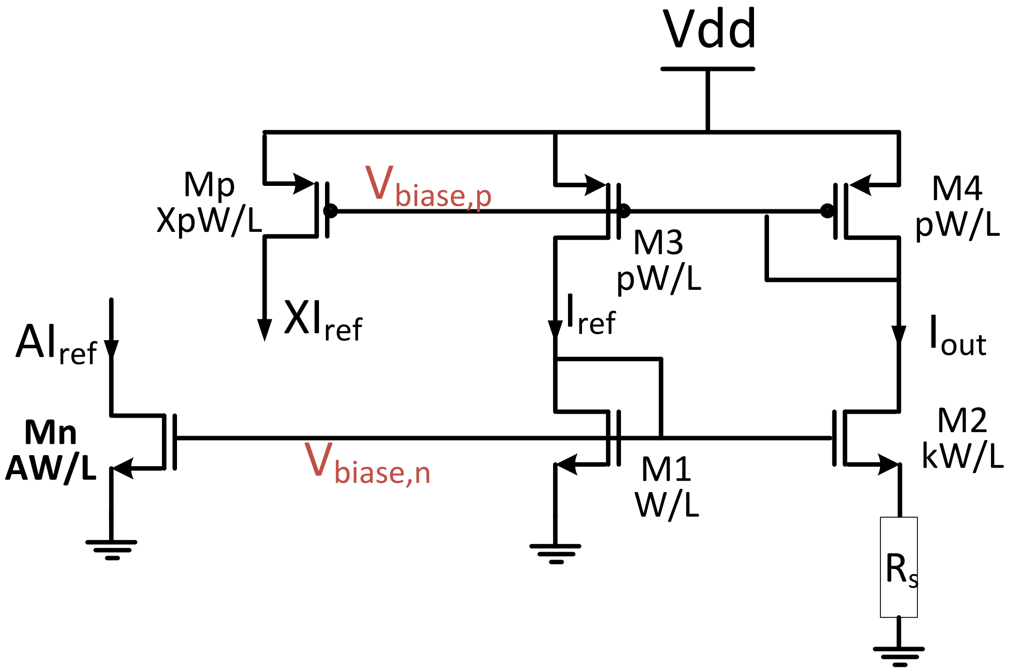
Ex: Temperature behavior of I_D in saturation

$$I_D = \frac{C_{ox} w/L}{2} \boldsymbol{\mu}(\boldsymbol{V_{GS}} - \boldsymbol{V_{T0}})^2$$



- At low V_G, the changes in V_{T0} dominate and the drain current increases with increasing temperature.
- At higher V_G, the mobility dominates and the drain current decreases with increasing temperature.

Exercise: Beta-multiplier (sensitivity temperature)



$$I_{out} = I_{ref} = \frac{2}{\beta_1 R_s^2}\left(1 - \frac{1}{\sqrt{k}}\right)^2$$

1. Give the relation between g_{m1} , g_{m2} and R_s if $k = 4$?
2. Analyze the variation of I_{out} with the temperature and determine $I_{out}(80°C)$ if $I_{out}(27°C)=10\mu A$ and $TC_{Rs} = 2000$ ppm/°C.

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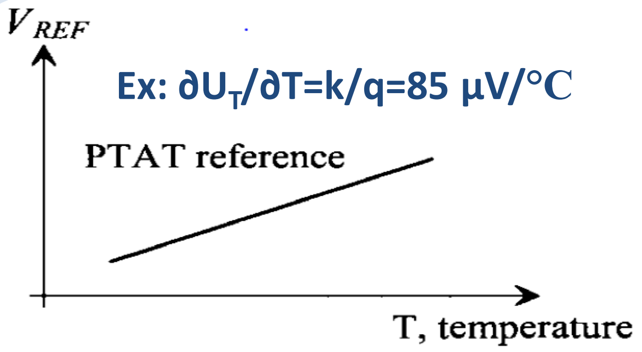
$$I_{out} = I_{ref} = \frac{2}{\beta_1 R_s^2}\left(1 - \frac{1}{\sqrt{k}}\right)^2$$

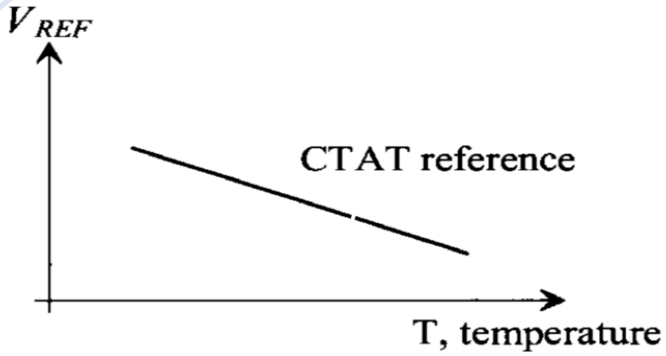
Temperature-Independent References

- Ideal I_{ref} and V_{ref} are PV**T**-independent
- Need two quantities having opposite TempCo: i.e. PTAT and CTAT



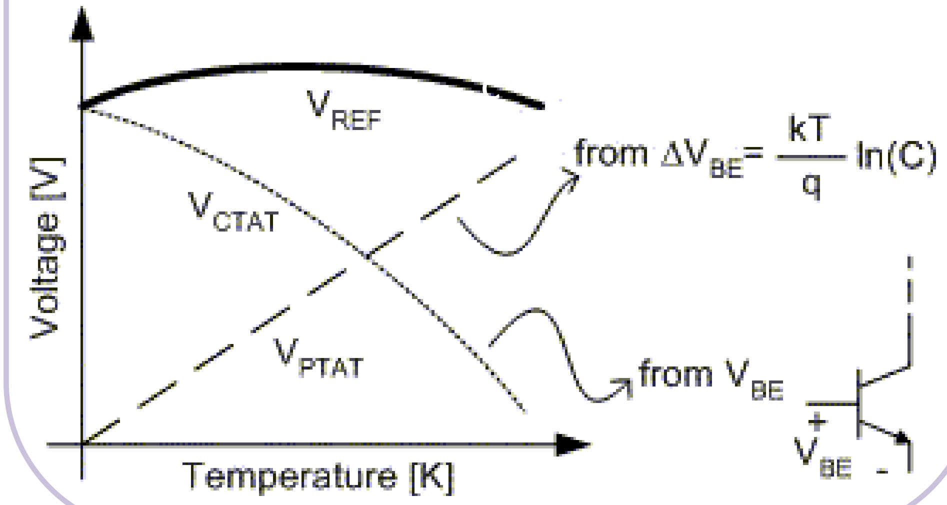
Ex: $\partial U_T/\partial T = k/q = 85\ \mu V/°C$

Proportional To Absolute Temperature



Complementary To Absolute Temperature

- T-independent reference (bandgap) are Generated by adding PTAT and CTAT references with proper weighting. (present in every chip)



CTAT Ex:

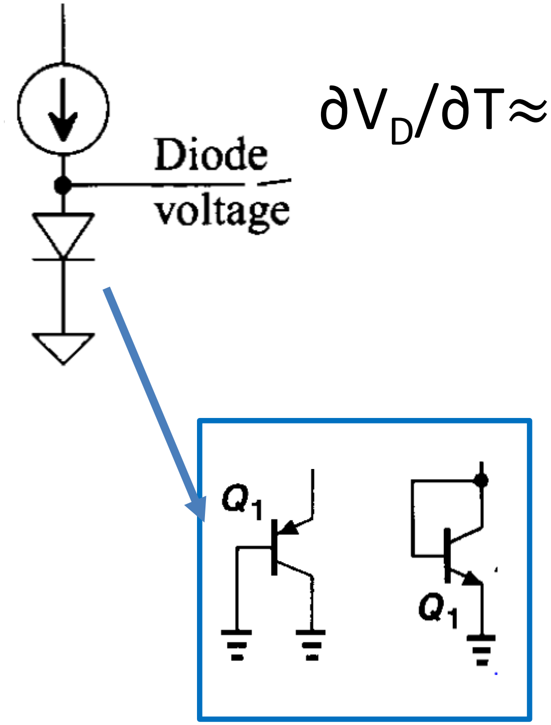
$\partial V_{BE}/\partial T \approx \partial V_D/\partial T \approx -1.6$ mV/°C;

$\partial V_{T0}/\partial T \approx -0.6$ mV/°C;

$\partial kp/\partial T \approx -\ kp\ 1.5/T$ (T in °K)

Negative-TC Ref(CTAT)

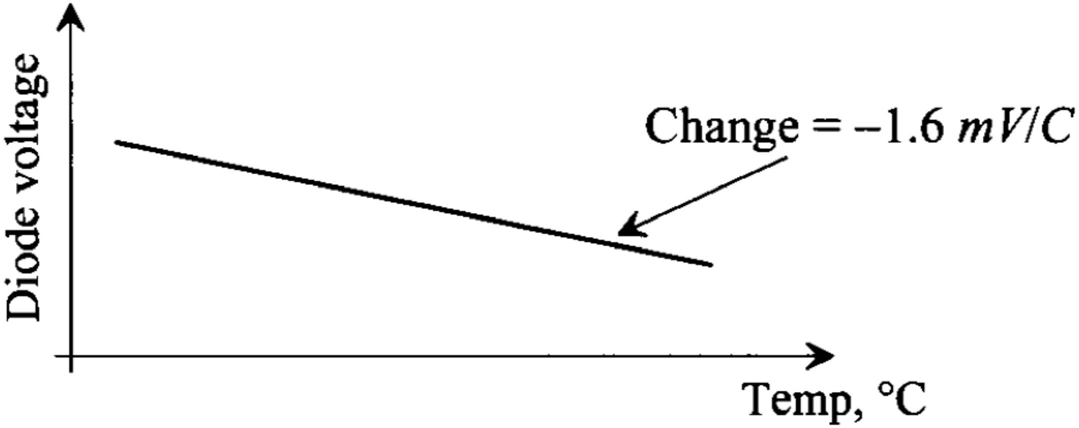
- Base-emitter Voltage of Bipolar (i.e. forward voltage of a diode) exhibits a negative TC (CTAT).



$\partial V_D/\partial T \approx -1.6\, mV/°C$

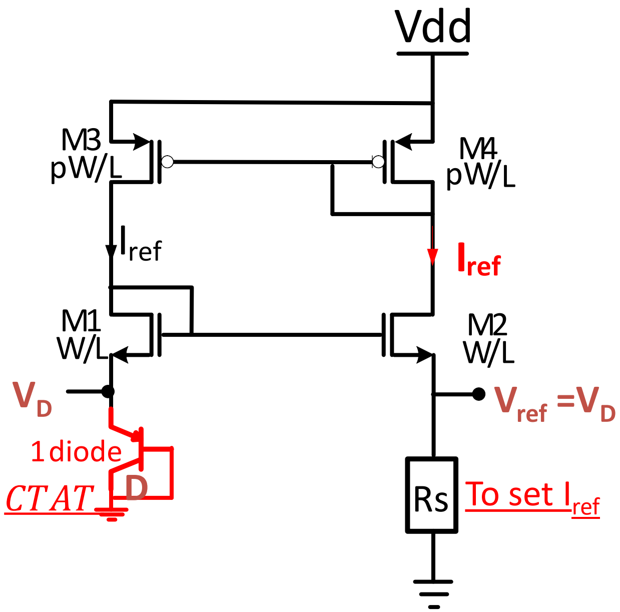
$I_D = I_S.\exp(V_D/U_T)$, $U_T = kT/q$

$V_D = U_T.\mathrm{Ln}(I_D/I_s)$



Note: Bipolar transistors give the most reproducible and **easily tunable positive** and negative TC references and temp-independent references.

Conceptual generation of CTAT-Ref:
Diode-referenced self-biasing circuit (CTAT)



- *pMOS mirror forces the same current through each branch.*
- *nMOS mirror forces the source voltages of M1 et M2 to be the same*
- *The temperature Coefficient of* V_{ref}

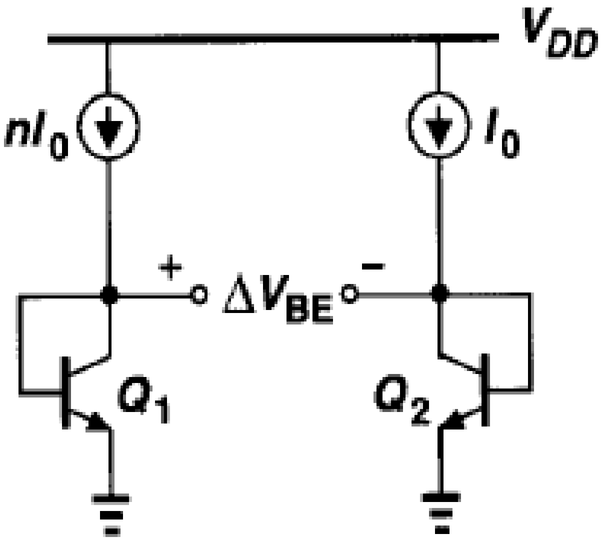
$$TC(V_{ref}) = TC(V_D) \approx \frac{-1{,}6mV/°C}{0{,}7V} \; CTAT$$

- We can set the value of I_{ref} by choosing the right value of R_s

$$I_{ref} = \frac{\overbrace{V_{ref}}^{V_D}}{R_s} = \frac{U_T \ln\left(\frac{I_{ref}}{I_s}\right)}{R_s} \rightarrow R_s = \frac{U_T}{I_{ref}} \ln\left(\frac{I_{ref}}{I_s}\right)$$

$$\boxed{TC(I_{ref}) = TC(V_D) - TC(R_s) \rightarrow CTAT \; if \, R_s is \; PTAT}$$

Conceptual generation of Positive-TC Ref(PTAT)



- *The difference between the base-emitter voltages of two BJTs operating at unequal currents is known as PTAT.*

$$\Delta V_{BE} = U_T ln\left(\frac{nI_o}{I_s}\right) - U_T ln\left(\frac{I_o}{I_s}\right)$$

$$= U_T ln(n) = \frac{kT}{q} ln(n)$$

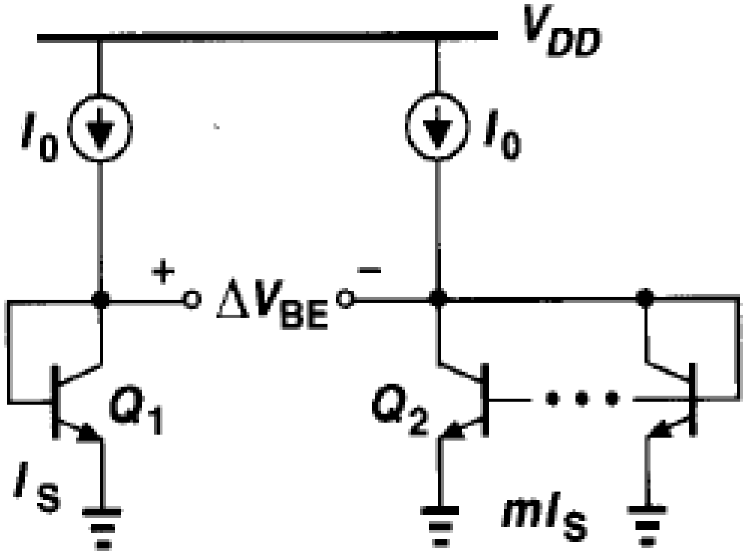
$$\boxed{\frac{\partial \Delta V_{BE}}{\partial T} = ln(n)\frac{\partial U_T}{\partial T}}$$

$$= ln(n)\,85\frac{\mu V}{°C} \quad \rightarrow tunable\ PTAT$$

- *The weighting of ΔV_{BE} is tunable through n.*

Conceptual generation of Positive-TC Ref (PTAT): version 2

- *The difference between the base-emitter voltages of two BJTs with unequal sizes is also known as PTAT.*



$$\Delta V_{BE} = U_T ln\left(\frac{I_o}{I_s}\right) - U_T ln\left(\frac{I_o}{mI_s}\right)$$

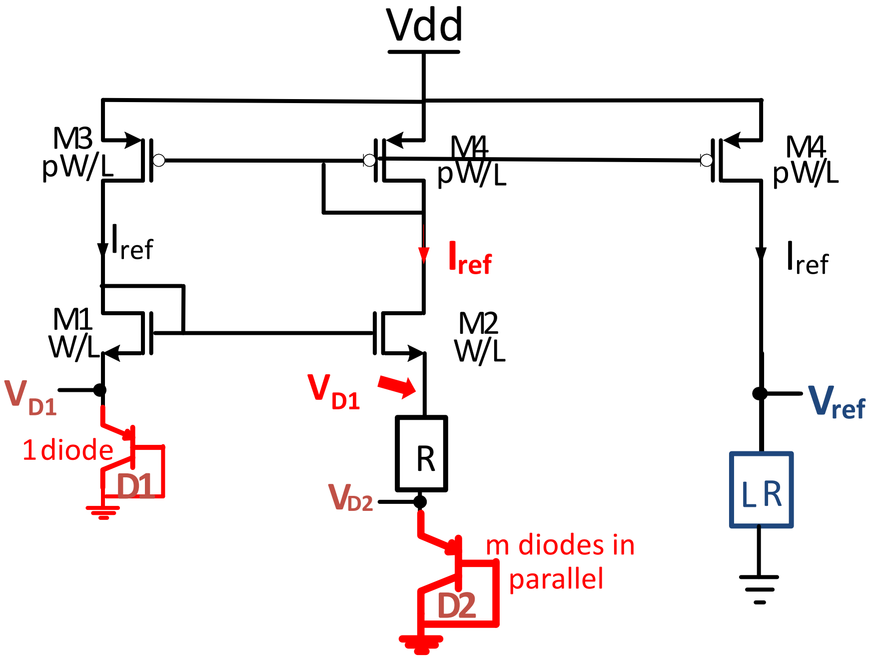
$$= U_T ln(m) = \frac{kT}{q} ln(m)$$

$$\boxed{\frac{\partial \Delta V_{BE}}{\partial T} = ln(m)\frac{\partial U_T}{\partial T} = ln(m)\,85\,\frac{\mu V}{°C} \rightarrow tunable\ PTAT}$$

- *The weighting of ΔV_{BE} is tunable trough m.*

- *ΔV_{BE} is a floating voltage*
- *Ground-referenced PTAT voltage?*

Ground-referenced PTAT-Ref



- *The difference between the base-emitter voltages of two BJTs can be achieved through a resistor:*

$$\Delta V_D = \overbrace{V_{D1}}^{V_{S(M2)}} - V_{D2} = U_T ln(m) = RI_{ref}$$

$$I_{ref} = \frac{U_T ln(m)}{R}$$

$$\boxed{V_{ref} = LRI_{ref} = U_T L ln(m)}$$

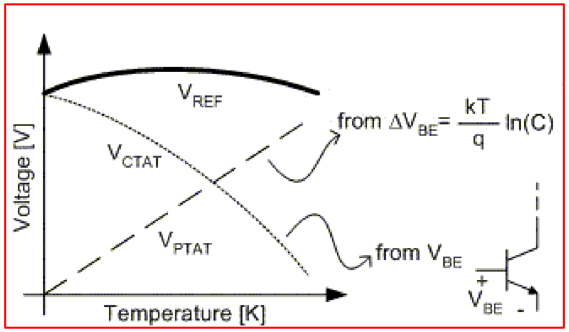
→ GND-referenced tunable PTAT

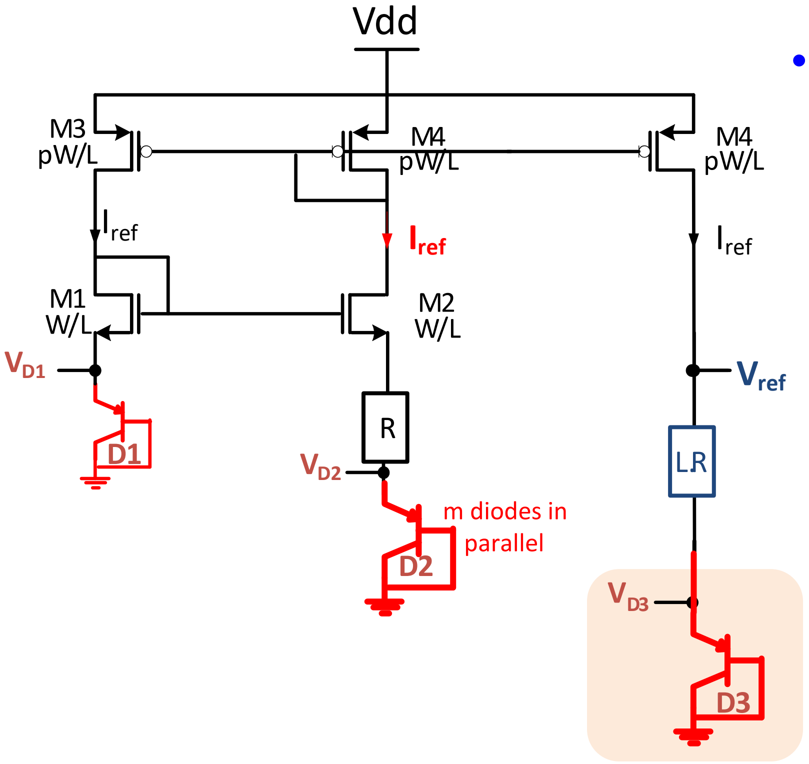
$$\boxed{\frac{\partial V_{ref}}{\partial T} = L\ ln(m)\frac{\partial U_T}{\partial T} = L\ ln(m)\ 85\,\frac{\mu V}{°C}}$$

- *The value of I_{ref} is set by choosing the right value of R as:*

$$I_{ref} = \frac{V_{D1} - V_{D2}}{R} = \frac{U_T \ln(m)}{R} \rightarrow \mathrm{R} = \frac{U_T \ln(m)}{I_{ref}}$$

Band Gap Reference Design





- *The bandgap reference (BGR) is formed by adding a diode D_3 (i.e., CTAT) to a PTAT reference. The reference voltage is then the sum of tunable PTAT and CTAT voltages:*

$$V_{ref} = LRI_{ref} + V_{D3} = \overbrace{U_T L \ln(m)}^{PTAT} + \overbrace{V_{D3}}^{CTAT}$$

$$\frac{\partial V_{ref}}{\partial T} = L \ln(m) \underbrace{\frac{\partial U_T}{\partial T}}_{+85\frac{\mu V}{^\circ C}} + \underbrace{\frac{\partial V_{D3}}{\partial T}}_{-1,6\frac{mV}{^\circ C}}$$

- *L could be tuned to have* $\frac{\partial V_{ref}}{\partial T} = 0$

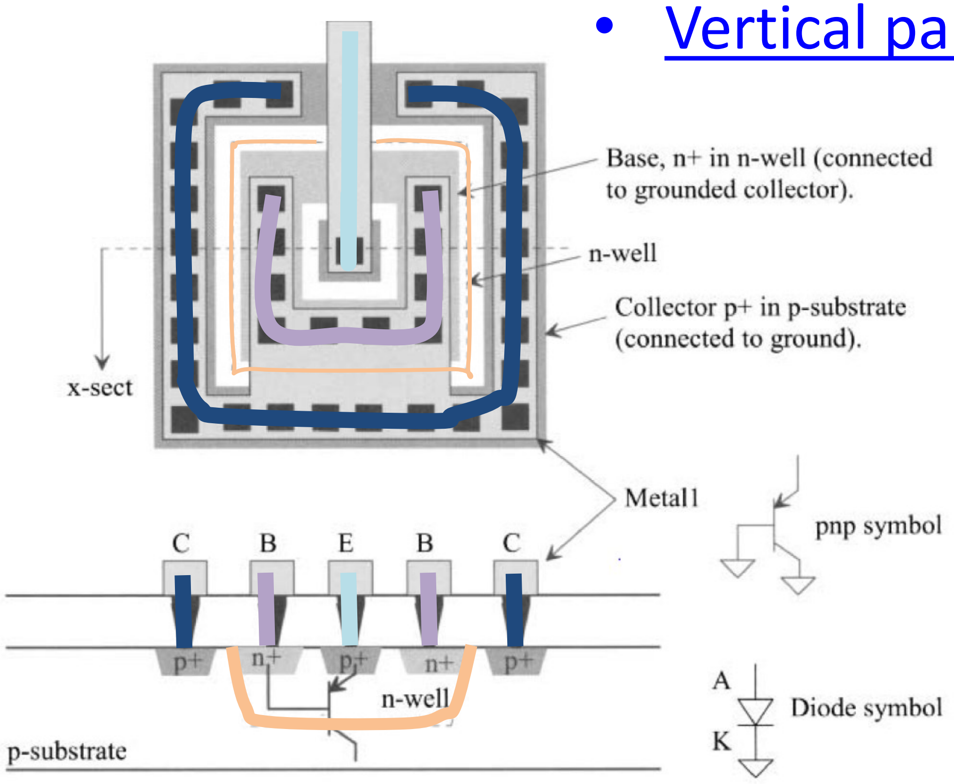
$$\rightarrow \; L = \frac{1,6}{\ln(M)85\;10^{-3}} \approx 9 \text{ for M = 8}$$

- *Note that as for Beta Multiplier, the PTAT, CTAT and Bandgap circuits based on the self-biasing structure require start-up circuits.*

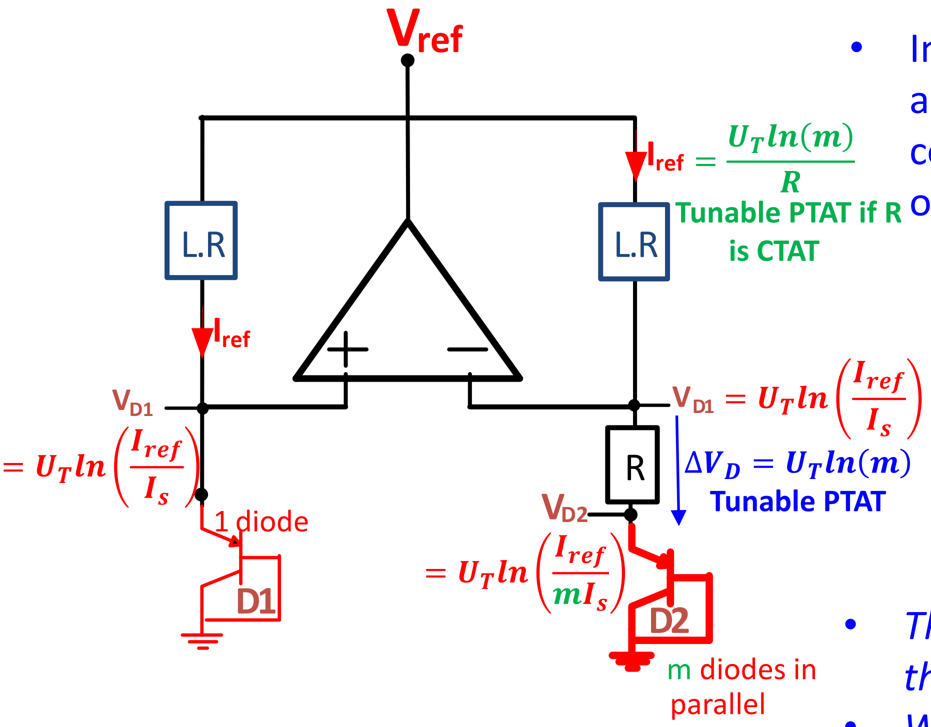
Bipolar implementation in CMOS process

- *Our derivation of a temperature-independent voltage relies on the exponential characteristics of Bipolar for both PTAT and CTAT.*
- *We must therefore seek structures in a standard CMOS technology that exhibit such characteristics.*

- <u>Vertical parasitic pnp Bipolar</u>



Alternative Bandgap for Low-Voltage ICs

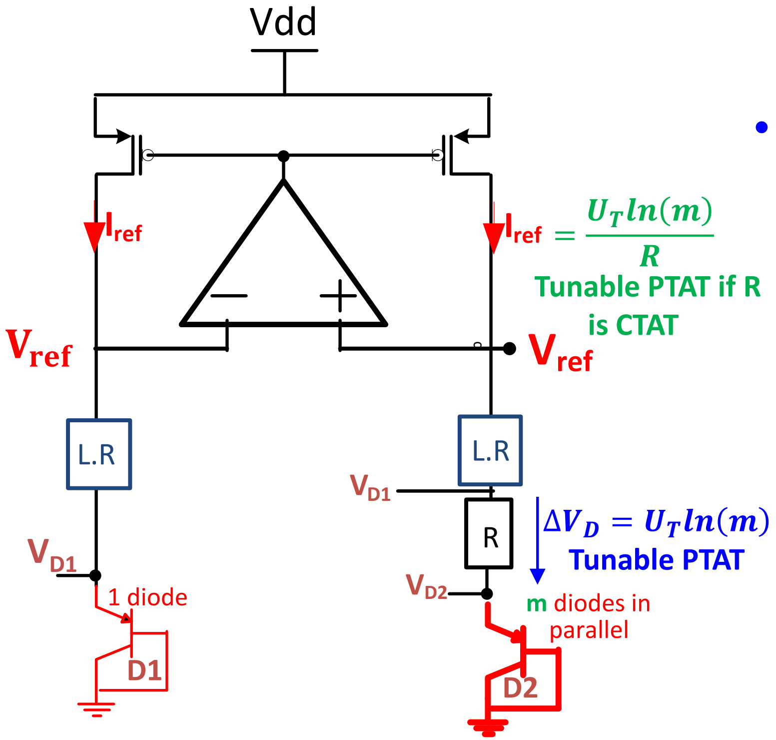


- Instead of using a self-biasing structure, we can use an amplifier to hold the voltage across the resistors (LR) constant and thus force the current through each branch of the reference to be the same.

$$V_{ref} = (L+1)RI_{ref} + V_{D2}$$
$$= U_T(L+1)\, ln(m) + V_{D2}$$

- *The benefit of this topology over the other topologies is that we can generate higher V_{ref} (closer to VDD).*
- *While its drawback is that the amplifier must be capable of driving a resistive load (which requires a current amplifier at the output stage).*

Alternative Bandgap for Low-Voltage ICs



- *This alternative avoids the resistive load since the amplifier drives the oxide capacitances of the pMOS amplifier.*

$$V_{ref} = (L+1)RI_{ref} + V_{D2}$$
$$= (L+1)\ ln(m)U_T + V_{D2}$$